IN THE CLAIMS:

1. (Amended) In a process of fabricating a narrow channel width PMOSFET device, the improvement of affecting reduction of negative bias temperature instability by use of F_2 side wall implantation and subsequent high density plasma fill of a STI, comprising:

a) forming a shallow trench isolation (STI) region in a substrate;

b) forming a gate on a gate oxide in said substrate;

c) forming a liner layer in said shallow trench isolation region and subjecting said liner layer to oxidation to form a STI liner oxidation layer;

d) implanting F_2 into side walls of said STI liner oxidation layer at a large tilted angle with reference to the Y axis in sufficient amounts to affect reduction of negative bias temperature instability after a high density plasma fill of said STI F_2 implanted liner oxidation layer; and

e) filling the STI F_2 implanted structure from step d) with a high density plasma (HDP) fill to affect reduction of negative bias temperature instability and enhance gate oxidation at the STI corner, in the narrow channel width PMOSFET device.

CORRECTED VERSION OF AMENDED CLAIM

1. (Amended) In a process of fabricating a narrow channel width PMOSFET device, the improvement of affecting reduction of negative bias temperature instability by use of F_2 side wall implantation and subsequent high density plasma fill of a STI, comprising:

a) forming a shallow trench isolation (STI) region in a substrate;

b) forming a gate on a gate oxide in said substrate;

c) forming a liner layer in said shallow trench isolation region and subjecting said liner layer to oxidation to form a STI liner oxidation layer;

d) implanting F_2 into side walls of said STI liner oxidation layer at a large tilted angle with reference to the Y axis in sufficient amounts to affect reduction of negative bias temperature instability after a high density plasma fill of said STI F_2 implanted liner oxidation layer; and

e) filling the STI F_2 implanted structure from step d) with a high density plasma (HDP) fill to affect reduction of negative bias temperature instability and enhance gate oxidation at the STI corner, in the narrow channel width PMOSFET device.